Sierra Components, Inc.

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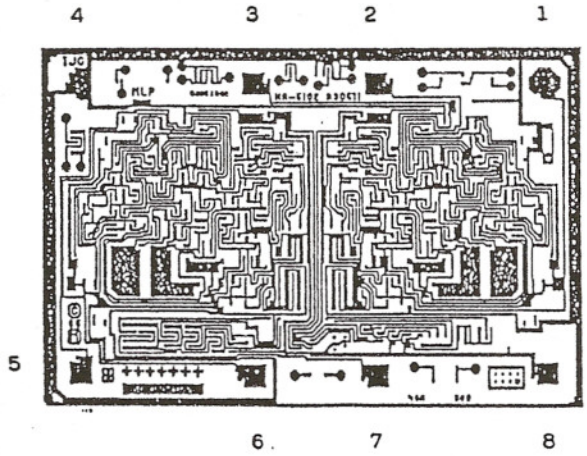
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD NO	FUNCTIONS
1	Output 1
2	Input 1-
3	Input 1+
4	V-
5	Input 2+
6	Input 2-
7	Output 2
8	V+

NOTE: Substrate may be connected to -V supply or may be left floating.

Topside Metal: Al
Backside: Si
Backside Potential: -
Mask Ref: -
Bond Pads: .004" min.

APPROVED BY: CD	**DIE SIZE: .098" x .067"**	**DATE: 7/26/02**
MFG: Harris	**THICKNESS: .019"**	**P/N: HA-5102-6**